Claims

[c1] 1. A flip-chip package substrate, comprising:
a plurality of patterned conductive layers sequentially stacked over each other;
at least one insulation layer between two neighboring conductive layers for isolating the conductive layers electrically such that the insulation layer alternates in position with the conductive layer; and
at least one conductive plug that passes through the insulation layer for connecting the conductive layers electrically,
wherein the uppermost conductive layer further includes:
a group of core bump pads; and
a plurality of bump pad rows sequentially laid outside the group of core bump pads, wherein one end of each of the bump pad rows is adjacent to the group of core bump pads with each bump pad row having a plurality of bump pads therein and the bump pad rows are selected from signal bump pad rows, power bump pad rows and ground bump pad rows.

[c2] 2. The package board of claim 1, wherein the group of core bump pads includes a plurality of core power bump pads and core ground bump pads.

[c3] 3. The package board of claim 1, wherein the bump pads in the power bump pad row are electrically connected together through the uppermost conductive layer.

[c4] 4. The package board of claim 1, wherein the bump pads in the ground bump pad row are electrically connected together through the uppermost conductive layer.

[c5] 5. The package board of claim 1, wherein the bump pads of the power bump pad row are electrically connected together through the second uppermost conductive layer.

[c6] 6. The package board of claim 1, wherein the bump pads of the ground bump pad row are electrically connected together through the second uppermost conductive layer.

[c7] 7. The package board of claim 1, wherein at least one signal bump pad row is

positioned between the power bump pad row and the ground bump pad row.

[c8] 8. A flip-chip package substrate, comprising:
a plurality of patterned conductive layers sequentially stacked over each other;
at least one insulation layer between two neighboring conductive layers for isolating the conductive layers electrically such that the insulation layer alternates in position with the conductive layer; and
at least one conductive plug that passes through the insulation layer for connecting the conductive layers electrically,
wherein the uppermost conductive layer further includes:
a group of core bump pads;
a plurality of inner bump pad rows sequentially laid outside a group of core bump pads, wherein a first end of each of the inner bump pad rows is adjacent to the group of core bump pads with each inner bump row having a plurality of inner bump pads therein, and the inner bump pad rows are selected from signal bump pad rows, power bump pad rows and ground bump pad rows; and
a plurality of outer bump pad rows sequentially laid outside a second end of each of the inner bump pad rows with each outer bump pad row having a plurality of outer bump pads thereon and the outer bump pad rows labeled sequentially as a first outer bump pad row, a second outer bump pad row and a third outer bump pad row from inside to outside, wherein the shortest distance between the neighboring outer bump pads within the second outer bump pad row is wide enough to permit the passage of at least one conductive trace, the shortest distance between the outer bump pad within the second outer bump pad row and the outer bump pad within the third outer bump pad row is wide enough to permit the passage of at least one conductive trace, and the shortest distance between the neighboring outer bump pads within the third outer bump pad row is wide enough to permit the passage of at least two conductive traces.

[c9] 9. The package board of claim 8, wherein the group of core bump pads includes a plurality of core power bump pads and core ground bump pads.

[c10] 10. The package board of claim 8, wherein the inner bump pads within the power bump pad row are electrically connected through the uppermost

conductive layer.

[c11] 11. The package board of claim 8, wherein the inner bump pads within the ground bump pad row are electrically connected through the uppermost conductive layer.

[c12] 12. The package board of claim 8, wherein the inner bump pads within the power bump pad row are electrically connected through the second uppermost conductive layer.

[c13] 13. The package board of claim 8, wherein the inner bump pads within the ground bump pad row are electrically connected through the second uppermost conductive layer.

[c14] 14. The package board of claim 8, wherein at least one signal bump pad row is positioned between the power bump pad row and the ground bump pad row.

[c15] 15. The package board of claim 8, wherein the outer bump pads are signal bump pads.

[c16] 16. A flip chip die having an active surface thereon, comprising:
a group of core die pads on the active surface; and
a plurality of die pad rows on the active surface sequentially laid outside the ground of core die pads such that one end of each of the die pad rows is adjacent to the group of core die pads and each die pad row includes a plurality of die pads therein, wherein the die pad rows are selected from signal die pad rows, power die pad rows and ground die pad rows.

[c17] 17. The flip chip of claim 16, wherein the group of core die pads includes a plurality of core power die pads and core ground die pads.

[c18] 18. The flip chip of claim 16, wherein at least one signal die pad row is positioned between the power die pad row and the ground die pad row.

[c19] 19. A flip chip die for joining with a flip-chip package substrate, wherein the flip-chip package substrate comprising:
a plurality of patterned conductive layers sequentially stacked over each other;

at least one insulation layer between two neighboring conductive layers for isolating the conductive layers electrically such that the insulation layer alternates in position with the conductive layer; and

at least one conductive plug passing through the insulation layer for electrically connecting the conductive layers,

wherein the upper most conductive layer further includes:

a group of core bump pads;

a plurality of inner bump pad rows sequentially laid outside a group of core bump pads, wherein a first end of each of the inner bump pad rows are adjacent to the group of core bump pads with each inner bump row having a plurality of inner bump pads therein, and the inner bump pad rows are selected from signal bump pad rows, power bump pad row and ground bump pad rows; and

a plurality of outer bump pad rows sequentially laid outside a second end of each of the inner bump pad rows with each outer bump pad row having a plurality of outer bump pads thereon and the outer bump pad rows labeled sequentially as a first outer bump pad row, a second outer bump pad row and a third outer bump pad row from inside to outside, wherein the shortest distance between the neighboring outer bump pads within the second outer bump pad row is wide enough to permit the passage of at least one conductive trace, the shortest distance between the outer bump pad within the second outer bump pad row and the outer bump pad within the third outer bump pad row is wide enough to permit the passage of at least one conductive trace, and the shortest distance between the neighboring outer bump pads within the third outer bump pad row is wide enough to permit the passage of at least two conductive traces; and

the flip chip die having an active surface thereon, comprising:

a group of core die pads on the active surface that corresponds in position to the group of core bump pads;

a plurality of inner die pad rows on the active surface that correspond to the inner bump pad row, wherein each inner die pad row has a plurality of inner die pads that correspond in position to the inner bump pads and the inner die pad rows are selected from signal die pad rows, power die pad rows and ground die pad rows; and

a plurality of outer layer die pad rows on the active surface that correspond in position to the outer bump pad rows, wherein each outer die pad row has a plurality of die pads that correspond in position to the outer bump pads.

Sub a1 >

[c20] 20. The flip chip of claim 19, wherein the group of core bump pads includes a plurality of core power bump pads and core ground bump pads and the group of core die pads includes a plurality of core powerbump pads and core ground die pads that correspond in position to the core power bump pads and core ground bump pads.

[c21] 21. The flip chip of claim 19, wherein at least one signal die pad row is positioned between the power die pad row and the ground die pad row.

[c22] 22. The flip chip of claim 19, wherein the outer die pads are signal die pads.

add a2 >